09/886,741

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Chan, et al.
Serial No. 09/886,741
Filing Date: June 21, 2001

Examiner: Unknown
Art Group: Unknown
Our file no. 00100.01.0068
Docket No. 0100680

Title: **MULTI-DIE MODULE AND METHOD THEREOF**

Assistant Commissioner for Patents
U.S. Patent and Trademark Office
Washington, D.C. 20231

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2-13-02 Karenina Oliver
Date *Karenina Oliver*

PRELIMINARY AMENDMENT

Dear Sir:

Please enter the following amendment into the above-identified application before examination on the merits thereof. Marked-up versions of the amendments presented below are provided in the corresponding exhibits at the end of this amendment.

IN THE DRAWINGS

Subject to the approval of the Examiner, it is respectfully requested that the enclosed substitute drawings, corresponding to FIG. 1, 4-6 and 9 replace the original drawings filed with the above-identified application. A copy of the drawings corresponding to FIG. 1, 4-6 and 9, with changes indicated in red, is also enclosed in Exhibit A.

IN THE SPECIFICATION

12/05/06 gb

Please replace paragraph beginning on page 4, line ~~17~~ 16 with the following:

FIG. 4 illustrates the partially completed multi-die module of FIG. 3, after unpackaged semiconductor die 110 has been encapsulated with encapsulation material 180. Some examples of encapsulation material 180 are epoxy, metal cap or silicon coatings. Encapsulation material 180 may be dry molded or liquid molded depending on the type of encapsulation material desired. At this stage, solder balls 160 may be added to the bottom of multi-die module substrate 140 to provide for future connection of the completed package module 100 (FIG. 1) to a circuit board and/or other system. In order to facilitate interchangeability with many standard packages,

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solder balls 160 may have a pitch of 1.27 millimeters, 1.0 millimeters, 0.80 millimeters, 0.75 millimeters, or any other pitch suitable for a desired application. It will be appreciated that solder balls may be added at other suitable times during the manufacturing process.

Please replace the paragraph beginning on page 5, line ~~10~~ 8 with the following:

FIG. 6 illustrates a heat sink 150 added on top of unpackaged semiconductor die 110 and packaged die 120 and 130 to aid in removing heat from the circuits. As illustrated, the distance "d" from the top of multi-die module substrate 140 to the top of packaged die 120 and 130 is substantially equal to the distance from the top of multi-die module substrate 140 to the top of the encapsulation material over unpackaged semiconductor die 110, which is referred to herein as the top of unpackaged semiconductor die 110. In at least one embodiment, distance "d" is about 1.3 millimeters. Making these distances the same facilitates effective use of heat sink 150, although heat sink 150 could be fabricated to account for any difference between the heights of various packaged and/or unpackaged die attached or mounted to multi-die module substrate 140. In various embodiments, heat sink 150 may be a thin strip of heat conductive material, a large heat sink with fins for added heat dissipation, or any other suitable type of heat sink.

Please replace the paragraph beginning on page 6, line ~~17~~ 4 with the following:

FIG. 9 shows packaged die 120 and 130 attached as already discussed. Note however, that the top of unpackaged semiconductor die 111 is not level with the tops of packaged die 120 and 130. Therefore, shim 190 is used to effectively raise the top of unpackaged die 111 to be even with the tops of packaged die 120 and 130, and thereby facilitate the use of a heat sink (not shown). Shim 190 may be composed of silicon, or another suitable heat conveying material. It will be appreciated that a shim such as shim 190 may be used on top of packaged die 120 and/or 130, instead of or in addition being used on top of unpackaged die 111 if needed.

IN THE CLAIMS

Please amend claims 6-7 and 9 to read as shown below by substituting the below claims for claims having the same number, and add claims 41-55 as follows. Pursuant to 37 C.F.R. §1.121, a marked-up version of the following claims is provided at the end of this Amendment as Exhibit C.

09/886,741

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Chan, et al.
Serial No. 09/886,741
Filing Date: June 21, 2001

Examiner: C. Chu
Art Unit: 2815
Our File No. 00100.01.0068
Docket No. ATI.0100680

Title: **MULTI-DIE MODULE AND METHOD THEREOF**

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Washington, D.C. 20231

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10-21-02 Patricia O'Donoghue
Date *Patricia O'Donoghue*

AMENDMENT UNDER 37 C.F.R. §1.111

Dear Sir:

This Amendment is being submitted in response to the Office Action dated August 14, 2002, relating to the above-identified application. Reexamination and reconsideration of said application are respectfully requested.

IN THE SPECIFICATION

Please amend the specification as provided below. Pursuant to 37 C.F.R. §1.121, a marked-up version of the following paragraph(s) is provided at the end of this Amendment as Exhibit A.

Please replace the paragraph beginning on page 3, line ~~22~~ 21 with the following: 11/05/06 JM

In the embodiment illustrated, package module 100 has unpackaged die 110 mounted on it, as well as packaged die 120 and 130. In at least one embodiment, unpackaged die 110 is a data processor, such as a general purpose processor or a graphics processor, and packaged die 120 and 130 are memory packaged in Chip Scale Packages (CSP) or stacked CSP memories. In other embodiments, unpackaged die 110 may be an additional processor such as an audio processor, a general purpose processor, a controller, etc., while packaged die 120 and 130 may be static random access memories (SRAM), dynamic random access memories (DRAM), read only memories (ROM), flash memories, electrically erasable programmable memories (EEPROMS), or any other suitable memory type or combination of types. In addition, packaged

die 120 and 130 may be processors of the same or a different type than unpackaged die 110. Various embodiments of the present invention may employ different combinations of unpackaged semiconductor die 110 and packaged semiconductor die 120 and 130, including the use of two unpackaged semiconductor die 110 and only one packaged semiconductor die 120, or multiple packaged semiconductor die 120 and 130 with no unpackaged semiconductor die 110.

Please replace the paragraph beginning on page 4, line ~~6~~ 5 with the following: 12/05/06 QB

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FIG. 2 illustrates a partially completed multi-die module. Multi-die module substrate 140 is shown with unpackaged semiconductor die 110 attached in preparation for wire bonding. In one embodiment, multi-die module substrate 140 is a built up substrate having four to six layers. In another embodiment, multi-die module substrate 140 is a Bizmalemide Triazine (BT) substrate having two to six layers. It will be appreciated that any suitable substrate may be employed according to the teachings set forth herein.

Please replace the paragraph beginning on page 4, line ~~12~~ 11 with the following: 12/05/06 QB

FIG. 3 illustrates the partially completed multi-die module of FIG. 2, but now bond wires 175 have been added to make an electrical connection between multi-die module substrate 140 and unpackaged semiconductor die 110. In at least one embodiment, bond wires 175 are made of a corrosion resistant material, such as gold, to resist corrosion, but other suitable wire types or similar means of electrical connection may be employed as desired.

Please replace the paragraph beginning on page ~~6~~ 5, line ~~1~~ 26 with the following: 12/05/06 QB

FIG. 8 illustrates another method of insulating electrical connections between unpackaged semiconductor die 111 and multi-die module substrate 140. Since all of the

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electrical connections are underneath unpackaged semiconductor die 111, there is no need for total encapsulation of unpackaged semiconductor die 111 to protect the electrical connections. Consequently, unpackaged semiconductor die 111 is underfilled with underfill material 170. Underfill material 170 may include, but is not limited to, ASEUA03 and ASEUA04 types of underfill materials.